Memory System Architecture Using Hardware-based Page Replacement

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Nowadays, high performance computing is getting more and more important by emerging applications like big-data and cloud computing. Although speed itself accounts for the performance of device is important, architectural support also takes a significant role. Owing to memory capacity limitation, besides, it is not possible to load every necessary data into main memory, causing continuous page swap between memory and storage which are apart from each other. The longer swap path walking through main memory and storage, the bigger waste of processor resource. Accordingly, we focus on improving swap performance of computing system by shortening data path. In this paper, we propose a new memory system architecture exploiting NAND flash memory included in memory system, where page replacement is managed by swap manager connected to DRAM and NAND flash memory. Thereby the processor is no longer required to manage any page fault caused by DRAM capacity. The overall structure is illustrated in Fig 1. We modified gem5 simulator[1] to support the proposed architecture, and set-up 128MB of main memory and plenty of swap area. Fig 2 shows normalized execution times for conventional and the proposed architecture for benchmarks which having different footprints. We observed the proposed architecture is at least twice as fast where DRAM capacity is insufficient.

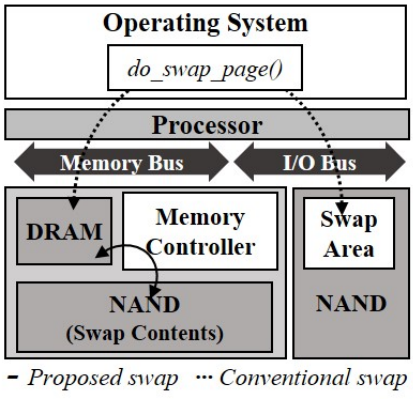

Fig 1. Structure of proposed system

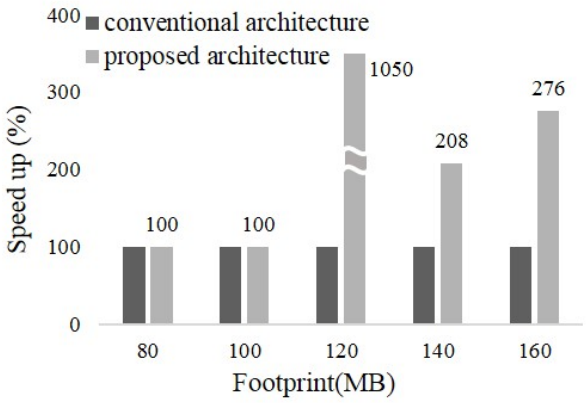

Fig 2. Simulation result

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[1] Binkert, N., Beckmann, B., Black, G., Reinhardt, S. K., Saidi, A., Basu, A & Wood, D. A. (2011). The gem5 simulator. ACM SIGARCH Computer Architecture News, 39(2), 1-7